DATA SHEET

PCF84C85A
Microcontroller with extended I/O

Product specification
Supersedes data of May 1994
File under Integrated Circuits, IC14

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead package
- 8 kbytes ROM
- 256 bytes RAM
- I^2C-bus interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 32 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - I^2C-bus
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Logic supply voltage: V_{DD} = 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C85A. The shared properties of the PCF84CxxxA family of microcontrollers are described in the *“PCD84xxxA family”* data sheet which should be read in conjunction with this publication.

The PCF84C85A is a general purpose CMOS microcontroller with emphasis on input/output. It provides 32 I/O port lines, 8 kbytes of program memory and 256 bytes of RAM. In addition to the 32 I/O port lines, the microcontroller provides an on-chip I^2C-bus interface. This two-line serial bus extends the microcontroller's capabilities when implemented with the powerful I^2C-bus peripherals.These include LCD drivers, telecom circuits, AD/DA converters, clock/calendar circuits, EEPROM and RAM and are listed in *“Data Handbook IC12, I^2C Peripherals”*.

The instruction set is based on that of the MAB8048 and is a sub-set of that listed in the *“PCF84CXXXA family”* data sheet.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	**DESCRIPTION**	**VERSION**
PCF84C85AP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT 129-1
PCF84C85AT	VSO40	plastic very small outline package; 40 leads	SOT 158-1

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

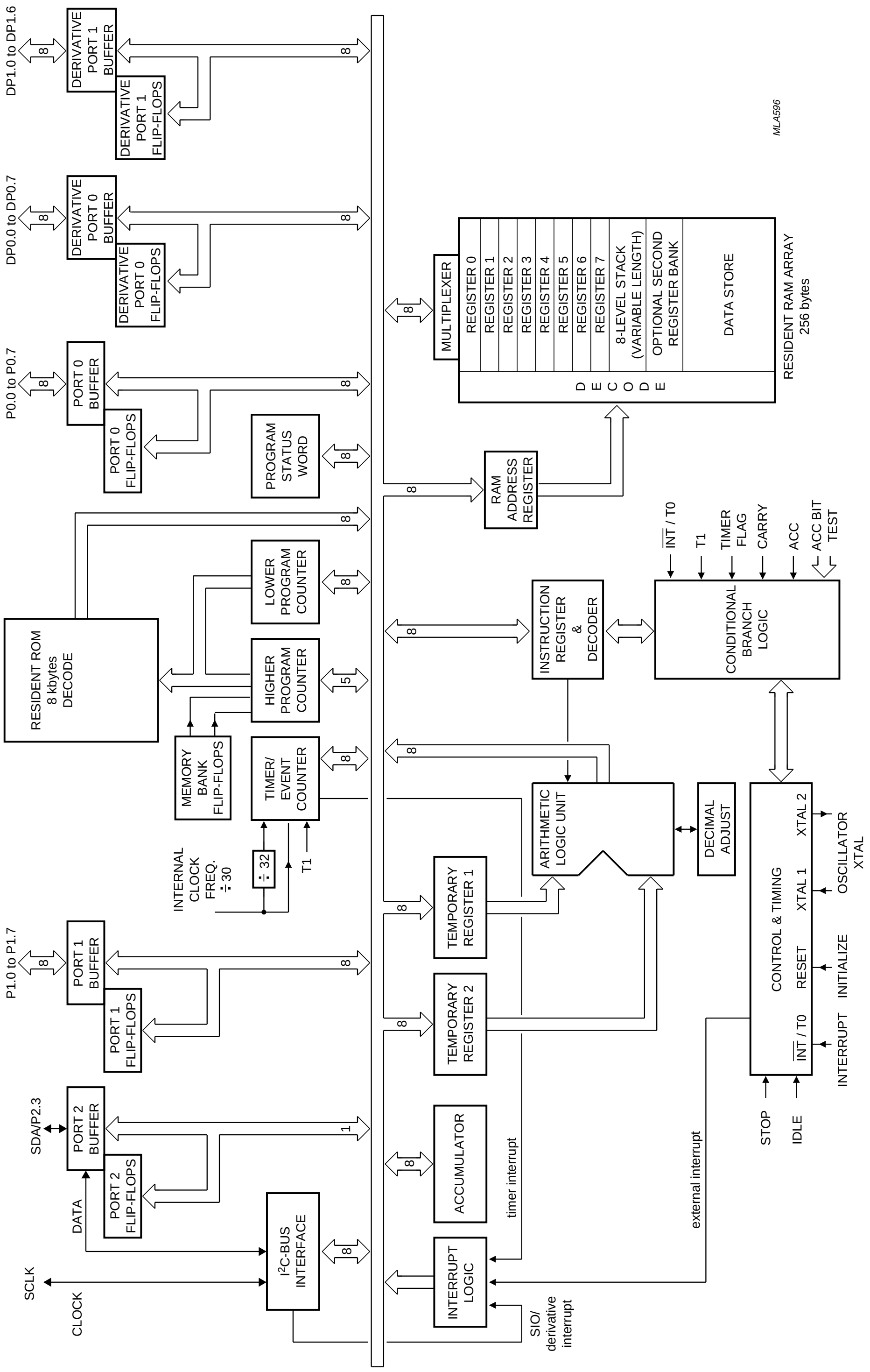


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

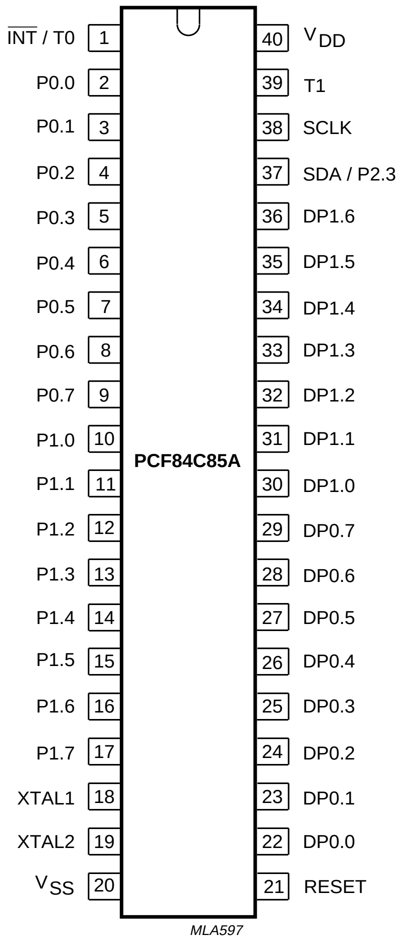


Fig.2 Pin configuration.

5.2 Pin description

Table 1 DIP40 and VSO40 packages.

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{INT}$/T0	1	I	Interrupt/Test 0
P0.0 to P0.7	2 to 9	I/O	8 bits of Port 0: 8-bit quasi-bidirectional I/O port
P1.0 to P1.7	10 to 17	I/O	8 bits of Port 1: 8-bit quasi-bidirectional I/O port
XTAL1	18	I	XTAL input: crystal oscillator/external clock input
XTAL2	19	O	XTAL output: crystal oscillator output
V_{SS}	20	P	ground
RESET	21	I	Reset input
DP0.0 to DP0.7	22 to 29	I/O	Derivative Port 0: quasi-bidirectional I/O port (8-bit)
DP1.0 to DP1.6	30 to 36	I/O	Derivative Port 1: quasi-bidirectional I/O lines (7-bit)
SDA/P2.3	37	I/O	bidirectional data line of the I^2C-bus interface; or Port 2 quasi-bidirectional I/O port (1 bit only)
SCLK	38	I/O	bidirectional clock line of the I^2C-bus interface
T1	39	I	Test 1: count input of 8-bit timer/event counter 1
V_{DD}	40	P	positive supply

6 PARALLEL PORTS

Of the standard quasi-bidirectional I/O ports, Port 2 is incomplete, providing only line SDA/P2.3 that is shared with the I^2C-bus interface. In addition to the standard ports, two derivative I/O ports are available:

- Derivative Port of 8 lines (DP0.0 to DP0.7)
- Derivative Port of 7 lines (DP1.0 to DP1.6).

Missing bits of incomplete ports, i.e. P2.0 to P2.2 and DP1.7, are fixed at zero in the corresponding registers.

7 INSTRUCTION SET

See *"PCF84CXXXA family"* data sheet for a complete description of the instruction set.

8 SUMMARY OF DERIVATIVE PORTS AND REGISTERS

Table 2 Derivative Ports.

DERIVATIVE ADDRESS	TYPE	REGISTER MNEMONIC	DESCRIPTION
00H	R	DP0L	Derivative Port 0 lines
01H	R	DP1L	Derivative Port 1 lines
02H	R/W	DP0FF	Derivative Port 0 flip-flops
03H	R/W	DP1FF	Derivative Port 1 flip-flops
04H	–	–	

Table 3 Derivative Registers.

REGISTER MNEMONIC	7	6	5	4	3	2	1	0
DP0L	D0.7	D0.6	D0.5	D0.4	D0.3	D0.2	D0.1	D0.0
DP1L	0	D1.6	D1.5	D1.4	D1.3	D1.2	D1.1	D1.0
DP0FF	F0.7	F0.6	F0.5	F0.4	F0.3	F0.2	F0.1	F0.0
DP1FF	0	F1.6	F1.5	F1.4	F1.3	F1.2	F1.1	F1.0

9 ROM MASK OPTIONS

ROM CODE	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 8 kbytes.		
Port Output			
P0.0 to P0.7	standard	open-drain	push-pull
P1.0 to P1.7	standard	open-drain	push-pull
SDA/P2.3	–	open-drain	–
DP0.0 to DP0.7	standard	open-drain	push-pull
DP1.0 to DP1.7	standard	open-drain	push-pull
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.7	set	reset	–
SDA/P2.3	set	–	–
DP1.0 to DP1.7	set	reset	–
DP2.0 to DP2.2	set	reset	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. See *"Data Handbook IC14, Section: Handling MOS devices".*

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current (V_{SS})	–50	+50	mA
T_{stg}	storage temperature range	–65	+150	°C
T_j	operating junction temperature	–	90	°C

12 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage	see Fig. 3	2.5	–	5.5	V
I_{DD}	operating supply current	note 1; see Figs 4 and 5				
		V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL})	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	2.5	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	note 1; see Figs 6 and 7				
		V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL})	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	V_{DD} = 2.5 V; notes 1 and 2; see Fig.8	–	1.2	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Outputs						
I_{OL}	LOW level output sink current; except SDA/P2.3 and SCLK	V_{DD} = 5 V; V_O = 0.4 V; see Fig.9	1.6	12	–	mA
I_{OL2}	LOW level output sink current; SDA/P2.3 and SCLK	V_{DD} = 5 V; V_O = 0.4 V; see Fig.10	3.0	12	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 5 V; V_O = 3.5 V; see Fig.11	–40	–100	–	µA
		V_{DD} = 5 V; V_O = 0 V; see Fig.11	–	–140	–400	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 5 V; V_O = 4.6 V; see Fig.12	–1.6	–7	–	mA
Oscillator (see Fig.13)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs, including XTAL2, open (typical values at 25 °C with crystal connected between XTAL1 and XTAL2).
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET and T1 at V_{SS}; $\overline{INT}$/T0 at V_{DD}; crystal connected between XTAL1 and XTAL2; open drain outputs connected to V_{SS}; all other outputs open.

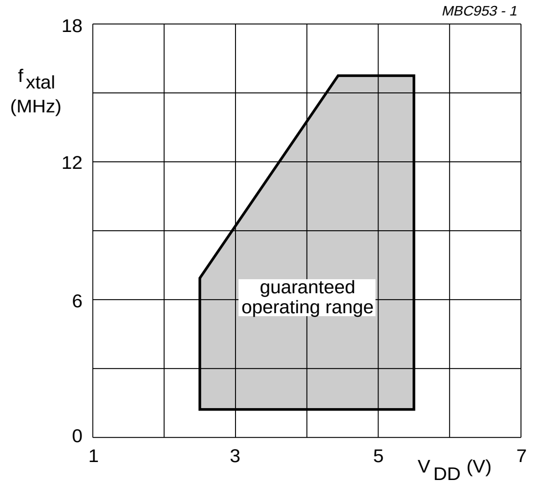
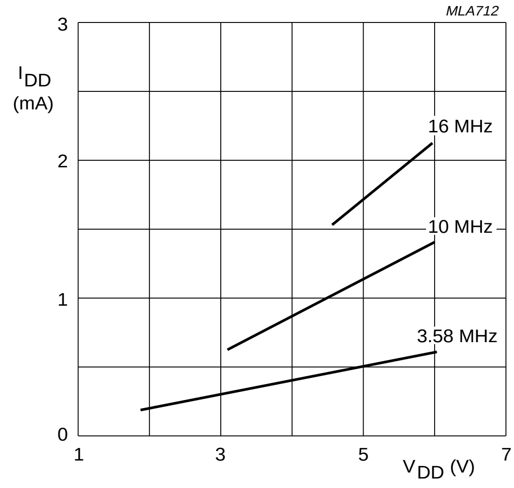
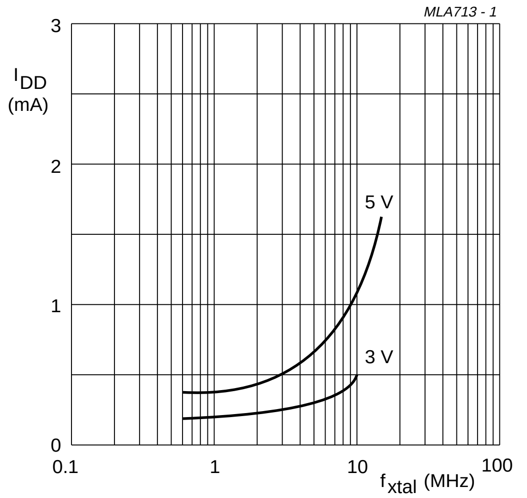


Fig.3 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



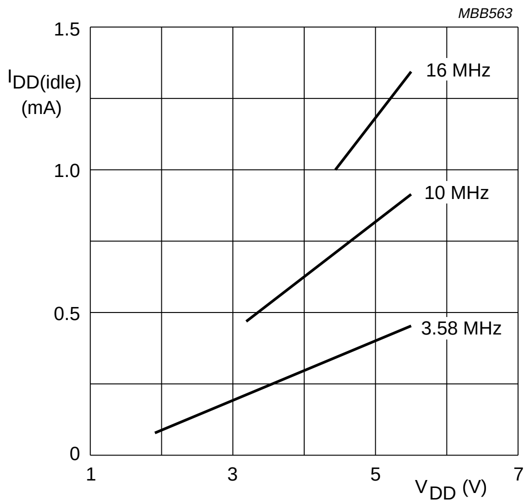
Supply current based on optimal oscillator selection.

Fig.4 Typical operating supply current (I_{DD}) as a function of operating supply voltage (V_{DD}).



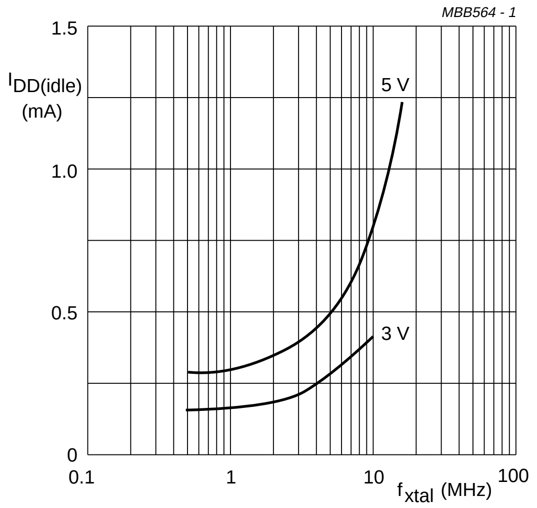
Supply current based on optimal oscillator selection.

Fig.5 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Supply current based on optimal oscillator selection.

Fig.6 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of operating supply voltage (V_{DD}).



Supply current based on optimal oscillator selection.

Fig.7 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).

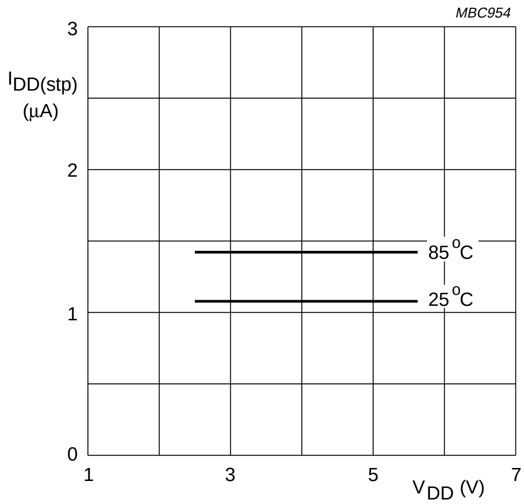
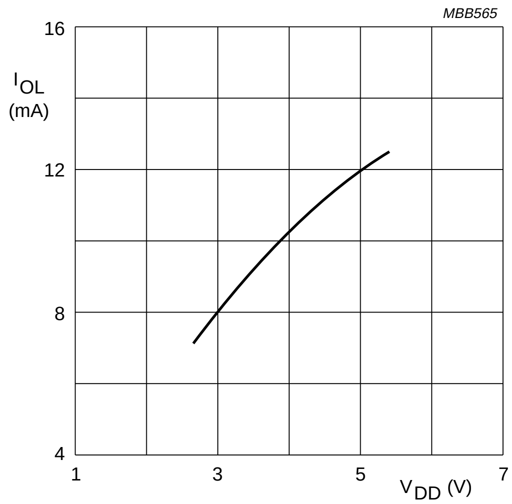


Fig.8 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of operating supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.9 Typical LOW level output sink current (I_{OL}) as a function of operating supply voltage (V_{DD}).

V_O = 0.4 V.

Fig.10 Typical LOW level output sink current for SDA/P2.3 or SCLK (I_{OL2}) as a function of operating supply voltage (V_{DD}).

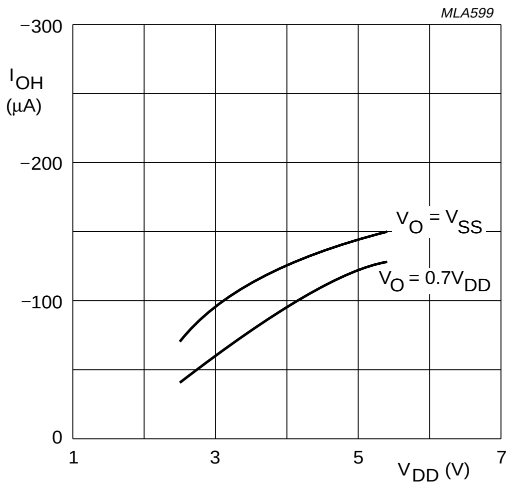
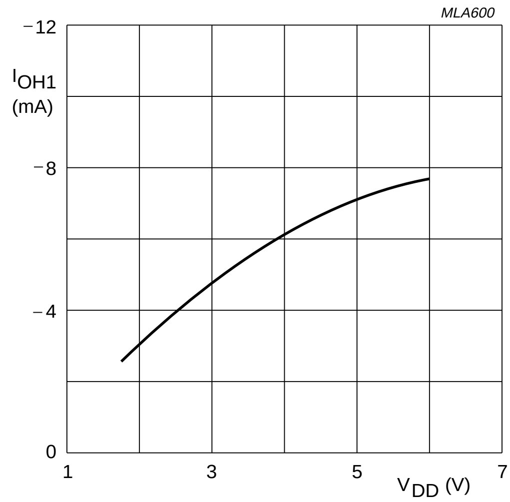


Fig.11 Typical HIGH level pull-up output source current (I_{OH}) as a function of operating supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.12 Typical HIGH level push-pull output source current (I_{OH1}) as a function of operating supply voltage (V_{DD}).

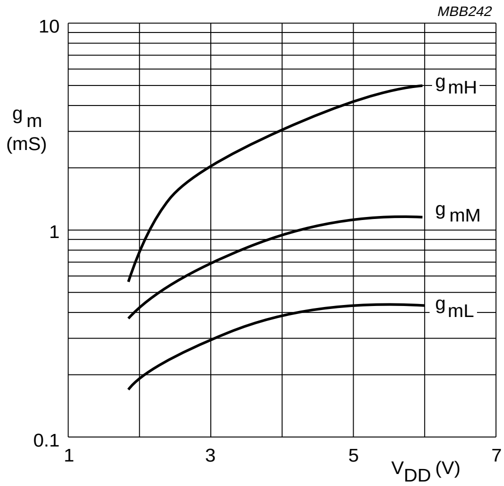


Fig.13 Typical transconductance (g_m) as a function of operating supply voltage (V_{DD}) for the options g_{mL}, g_{mM} and g_{mH}.

13 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
f_{xtal}	clock frequency	see Fig.3	1	–	16	MHz

Table 4 I^2C-bus timing (see Figs 14 and 15)

SYMBOL	PARAMETER	INPUT (see Fig.14)	OUTPUT (see Fig.15; note 1)
SCLK			
$t_{HD;STA}$	START condition hold time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF + 9}{2 \times f_{xtal}}$
t_{LOW}	SCLK LOW time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF - 3}{2 \times f_{xtal}}$; note 2
t_{HIGH}	SCLK HIGH time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF + 3}{2 \times f_{xtal}}$; note 2
t_{RC}	SCLK rise time	≤1 µs	≤1 µs; note 3
t_{FC}	SCLK fall time	≤0.3 µs	≤0.1 µs; note 4
SDA			
t_{BUF}	bus free time	$\geq \frac{14}{f_{xtal}}$	≥4.7 µs; note 5
$t_{SU;DAT}$	data set-up time	≥250 ns	$\geq \frac{15}{f_{xtal}}$; note 6
$t_{HD;DAT}$	data hold time	≥0	$\geq \frac{9}{f_{xtal}}$
t_{RD}	SDA/P2.3 rise time	≤1 µs	≤1 µs; note 3
t_{FD}	SDA/P2.3 fall time	≤0.3 µs	≤0.1 µs; note 4
$t_{SU;STO}$	STOP condition set-up time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF - 3}{2 \times f_{xtal}}$

Notes

1. DF stands for Division Factor: the divisor of f_{xtal} (see *“PCF84CXXXA family”* data sheet).
2. Values given for ASC = 0; for ASC = 1: $t_{HIGH} = \frac{3\,(DF + 1)}{4 \times f_{xtal}}$; $t_{LOW} = \frac{DF - 3}{4 \times f_{xtal}}$
3. Determined by I^2C-bus capacitance (C_b) and external pull-up resistor.
4. At maximum allowed I^2C-bus capacitance C_b = 400 pF.
5. Determined by program.
6. If $t_{LOW} < \frac{24}{f_{xtal}}$, $t_{SU:DAT} \geq \frac{t_{LOW} - 9}{f_{xtal}}$, independent of ASC.

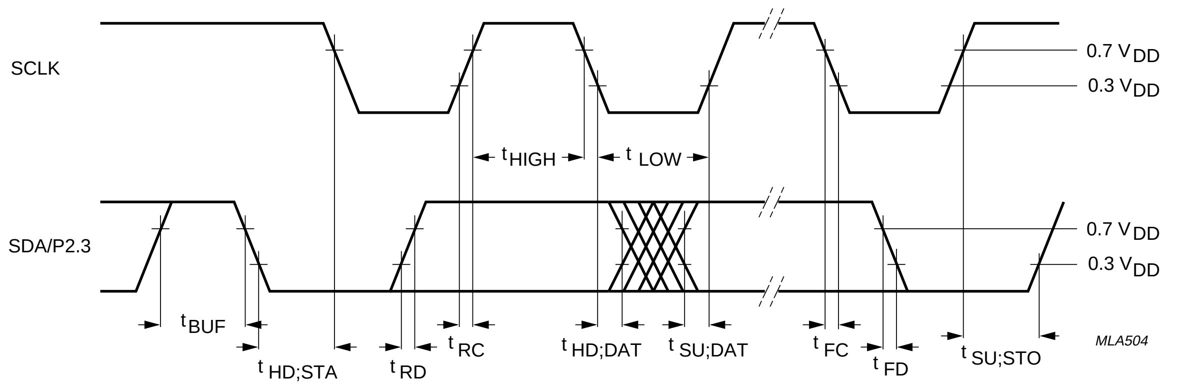


Fig.14 Slave SCLK and receiver SDA/P2.3 timing (SCLK and SDA/P2.3 are inputs).

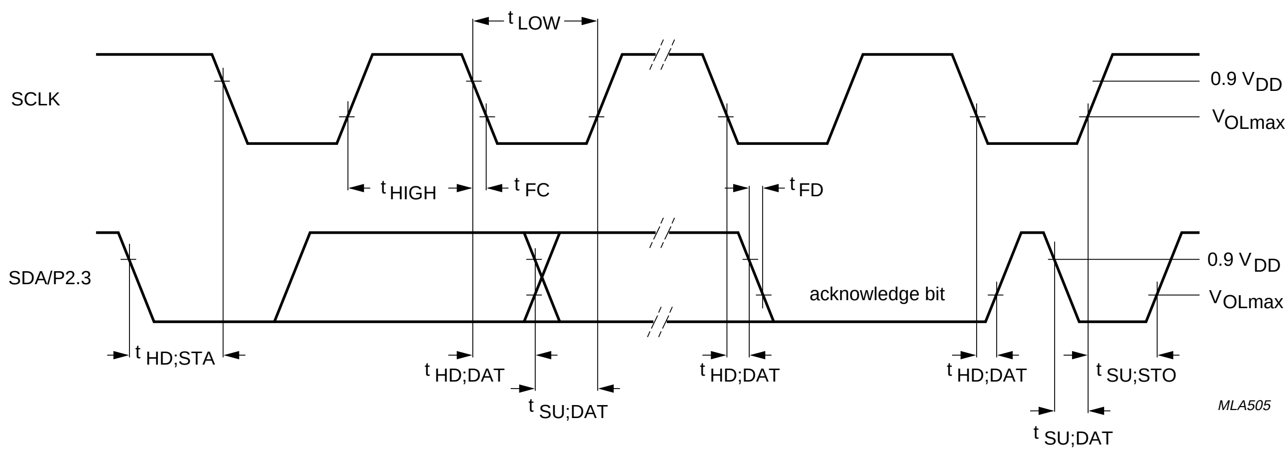
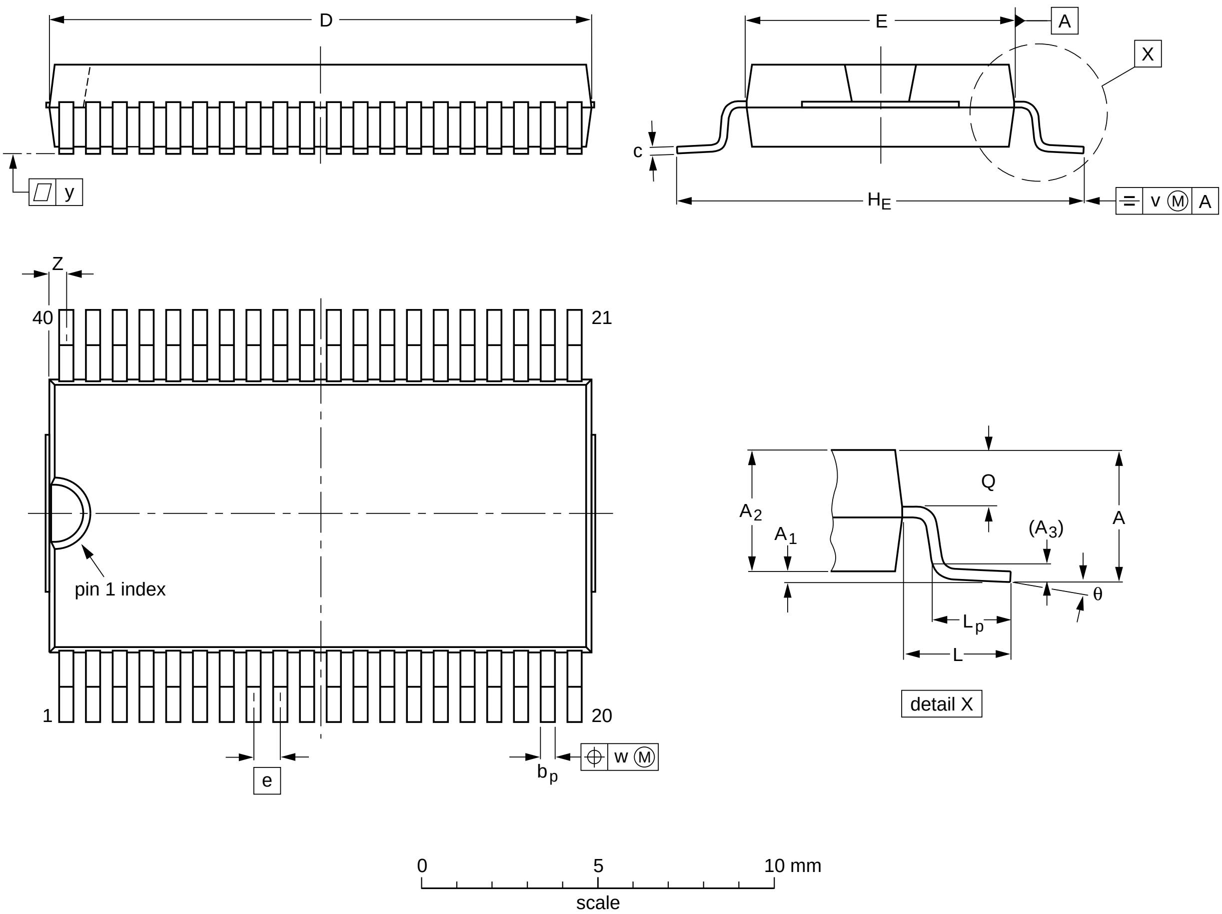


Fig.15 Master SCLK and transmitter SDA/P2.3 timing (SCLK and SDA/P2.3 are outputs).

14 PACKAGE OUTLINES

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

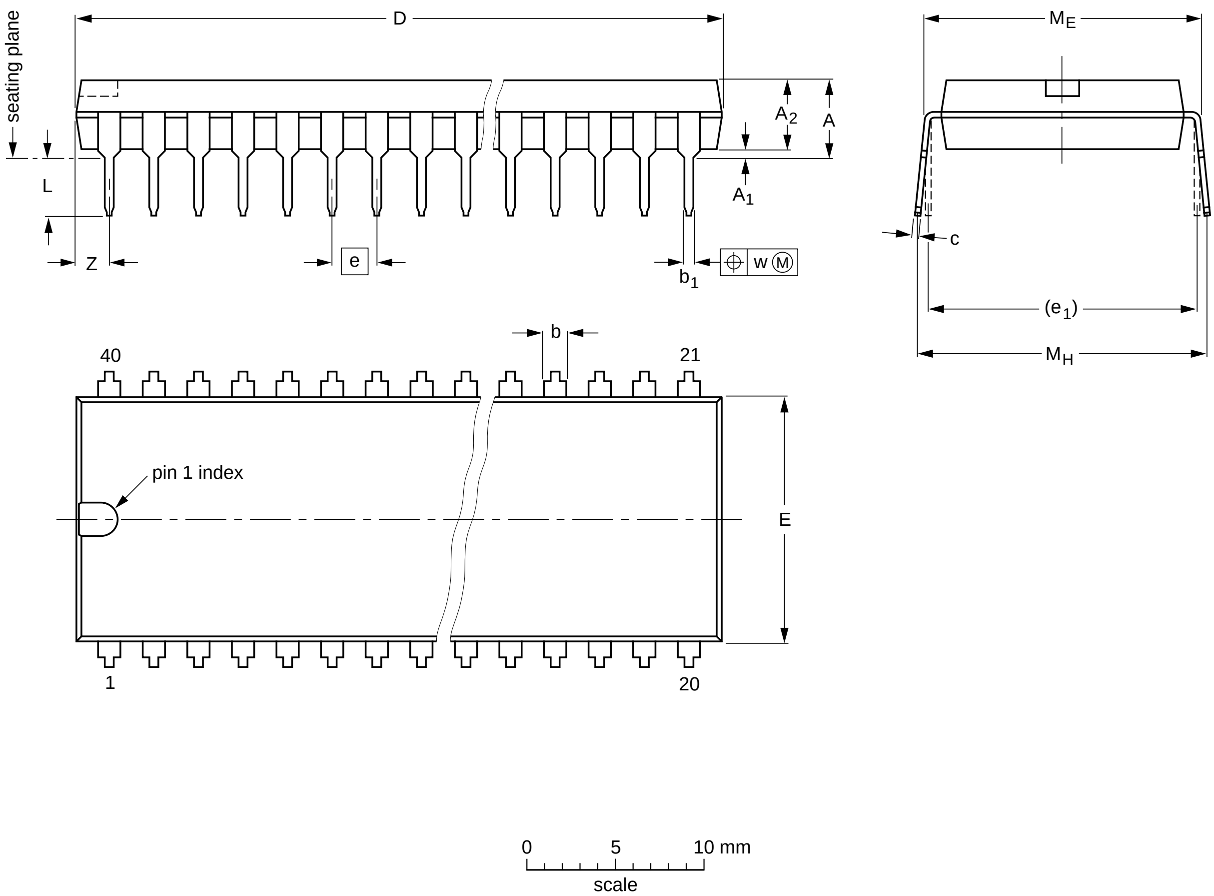
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 DIP

15.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.3 SO and VSO

15.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO and VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I^{2}C COMPONENTS

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Philips Semiconductors – a worldwide company

Argentina: see South America
Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466
Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101, Fax. +43 1 60 101 1210
Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773
Belgium: see The Netherlands
Brazil: see South America
Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102
Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381
China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700
Colombia: see South America
Czech Republic: see Austria
Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 1949
Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580/xxx
France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427
Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300
Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240
Hungary: see Austria
India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd. Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722
Indonesia: see Singapore
Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200
Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007
Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557
Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077
Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415
Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880
Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381
Middle East: see Italy
Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399
New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811
Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341
Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474
Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327
Portugal: see Spain
Romania: see Italy
Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 247 9145, Fax. +7 095 247 9144
Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. +65 350 2538, Fax. +65 251 6500
Slovakia: see Austria
Slovenia: see Italy
South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494
South America: Rua do Rocio 220, 5th floor, Suite 51, 04552-903 São Paulo, SÃO PAULO - SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 829 1849
Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107
Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 632 2000, Fax. +46 8 632 2745
Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2686, Fax. +41 1 481 7730
Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West Road, Sec. 1, P.O. Box 22978, TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444
Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793
Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707
Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461
United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421
United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381
Uruguay: see South America
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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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